## REMARKS

The present application contains claims 1-39. Claims 1, 3, 5, 15, 16, 18, 20, 24, 28, 32 and 39 have been amended in order to more clearly distinguish over the art of record.

The specification has been amended to cure certain minor informalities. No new matter has been added.

Figure 3 has been amended in order to conform legends in blocks 28 and 52 of Figure 3 with the specification. No new matter has been added.

It is noted that applicant's claim for domestic priority has been acknowledged.

The objections to claim 16, 18 and 20 are duly noted. Claims 16 and 18 have been amended to add the word "method" in accordance with the Examiner's suggestion. Similarly, claim 20 has been amended to recite a storing "method". For these reasons it is submitted that the objections to claims 16, 18 and 20 should be withdrawn.

Claims 5, 15, 28 and 36 have been rejected as failing to comply with the second paragraph of 35 U.S.C. Section 112. This rejection is respectfully traversed.

Claims 5, 15, 28 and 36 have been amended to remove the phrase "which may be corrupted." For these reasons it is submitted that claims 5, 15, 28 and 36 now comply with 35 U.S.C. Section 112 and that this rejection should be withdrawn.

Claims 1, 5, 24 and 32 have been rejected under 35 U.S.C. Section 101 because the claims consist of mathematical operations without practical application in the technological arts or simply manipulate abstract ideas or solves purely mathematical problems without any limitations or practical application. This rejection is respectfully traversed.

Firstly, these claims have been amended to recite a method employed by a decoder. Secondly, a major objective of the present invention is the ability to decode received signals by employing a memory used in conjunction with the calculation of forward and reverse metrics which significantly reduces the total memory capacity required. For example, note claim 1, as amended, which recites, at step (b) storing the metric calculations obtained in step (a) in a memory and wherein step (f) recites storing each of the forward metric calculations performed in the second stage into a memory location of said memory that a forward metric calculated during the first stages has been read out for use in an output calculation. This capability significantly reduces the memory capacity required to perform the necessary calculations and is set forth in the specification, for example, in paragraph [0011] appearing at page 3 of the specification and specifically the text found at lines 7 through 9. Claims 5, 24 and 32 have been amended in a similar fashion and for these reasons it is submitted that rejection of claim 1, 5, 24 and 32 based on 35 U.S.C. Section 101 should be withdrawn.

Claims 1-4, 15, 20-27, 32-35 and 39 have been rejected under 35 U.S.C. Section 102(e) as anticipated by Nakamura et al. (Patent '865).

This rejection is respectfully traversed.

The Examiner admits that Patent '865 does "not explicitly teach" a step of writing forward metric calculations during the second stage into a memory location that a forward metric calculated during the first stage has been read out for use in an output calculation and states that the step of reading and writing from and to a memory location or a storage is inherent to the system by virtue of the fact that the process of reading out and writing calculations to a storage according to a specific procedure is required and is commonly used by most error correction circuits. Applicant takes exception to the Examiner's position regarding inherency of reading and writing from/to a memory location and submits that in order to establish that the applicant's novel technique is inherent and commonly used, Applicant requests that a teaching of such capability employed in decoders and especially turbo decoders be shown to be a part of the prior art.

In addition, it is submitted that Patent '865 teaches away from this capability and that therefore providing this capability in Patent '865 is neither obvious nor inherent. Note, for example, Figure 2 which shows **separate** and **independent** forward path metric storing means 104 and backward path metric storing means 106. Note also Figure 8 which employs **separate** and **independent** forward path

metric storing means 104 and branch metric storing means 102, Figure 8 eliminating a backward path metric storing means.

In the embodiment shown in Figure 20 of Patent '865 there is only one calculating means, namely the forward path metric calculating means 202. There is no backward path metric calculating means or storing means. It should also be noted that the comparison results storing means 203 is independent of the differential value storing means 204.

In the embodiment shown in Fig. 23 **separate** and **independent** storing means, namely first coded sequence storing means 25 and second coded sequence storing means 26 are provided, the contents of storing means 25 being initially coupled to the first soft decision device 21a and thereafter when a completion of the soft decision output processing in the first soft decision device 21a is completed, the first coded sequence storing means 25 is connected to the second soft decision device 21b. There is no teaching of reading data used in one calculation into a memory location that data used in another calculation is being read out. Thus, it is submitted that Patent '865 teaches away from what the Examiner alleges to be an inherent and commonly used technique of "most of error correction circuits.". All of the claims 1-4, 15, 20-27, 32-35 and 39 recite limitations substantially similar to claim 1 and it is submitted that all of these claims patentably distinguish over Patent '865 for the same reasons set forth hereinabove with regard to claim 1.

Claims 5-14, 16-19, 28-31, 36-38 have been rejected under 35 U.S.C. Section 103(a) as unpatentable over Patent '865 in view of Xu (Patent '313). This rejection is respectfully traversed.

The Examiner admits that Patent '865 does not explicitly teach the step of reading a forward metric value from a memory for calculating an extrinsic value and relies upon Patent '313 for teaching an interative loop of the turbo decoder as increasing the magnitude of the LLR. Even assuming for the sake of argument that Patent '313 is combinable with Patent '865, the teachings lackings in Patent '865 are likewise lacking in Patent '313 and it is submitted that the combination of Patent '313 taken with Patent '865 lacks the features set forth in claims 5-14, 16-19, 28-31 and 36-38 for the same reasons set forth hereinabove with regard claims 1-4, 15, 20-27, 32-35 and 39. In view of the foregoing, it is submitted that claims 1-39 patentably distinguish over the art of record and reconsideration and allowance of these claims are earnestly solicited.

Favorable action is awaited.

If the Examiner believes that any additional minor formal matters need to be addressed in order to place this application in condition for allowance, or that a telephone interview will help to materially advance the prosecution of this application, the Examiner is invited to contact the undersigned by telephone at the Examiner's convenience.

Respectfully submitted,

Hepler et al.

By _____
Louis Weinstein
Registration No. 20,477

Volpe and Koenig, P.C.
United Plaza, Suite 1600
30 South 17th Street
Philadelphia, PA 19103
Telephone: (215) 568-6400
Facsimile: (215) 568-6499

LW/bbf
Enclosure

**Amendments to Drawings:**

The attached sheet of drawings includes changes to Fig. 3 This sheet, which includes Fig. 3, replaces the original sheet including Fig. 3. In Fig. 3, the legend in block 28 has been changed to "current_$\alpha$" and the legend in block 52 has been changed to "$\alpha$_ read".